REMARKS

Reconsideration of the application is requested.

Claims 1-6 are in the application. Claims 1, 3, and 5 have been amended. Claims 7-9 have been added.

In "Claim Objections" item 2 on page 2 of the above-identified final Office Action, the Examiner objected to claim 5 because of an informality in the preamble of claim 5. The Examiner's suggested correction has been made.

In "Claim Rejections - 35 USC § 112" item 4 on page 2 of the above-identified final Office Action, claims 5 and 6 have been rejected as being indefinite under 35 U.S.C. § 112, first paragraph.

More specifically, the Examiner states that "the specification, while being enabling for reading out a number of data items by the microprocessor from the reception FIFO … does not reasonably provide enablement for reading out data being currently written in the memory from the microprocessor." Applicant respectfully requests that the Examiner review the disclosure in the specification concerning FIG. 5 starting on page 18 and continuing to page 20, where the objected to process is described in d\more detail.

Moreover, it is believed that the amendments clarify that "said memory being arranged directly between said first data bus and said second data bus" as indicated in the Figures of the instant application.

Support for these changes may be found in the Figures 1 and 5 and on pages 2, 7, 8, and 18-20 of the specification of the instant application.

It is accordingly believed that the specification and the claims meet the requirements of 35 U.S.C. § 112, first paragraph. The above-noted changes to the claims are provided solely for clarification or cosmetic reasons. The changes are neither provided for overcoming the prior art nor do they narrow the scope of the claim for any reason related to the statutory requirements for a patent.

In "Claim Rejections - 35 USC § 103" item 6 on page 3 of the above-identified final Office Action, claims 1 and 2 have been rejected as being obvious over Applicant's Allegedly Admitted Prior Art (hereinafter **AAAPA**) in view of U.S. Patent No. 5,046,039 to *Ugajin, et al.* (hereinafter **UGAJIN**) under 35 U.S.C. § 103(a).

In "Claim Rejections - 35 USC § 103" item 7 on page 5 of the above-identified final Office Action, claims 3 and 4 have been rejected as being obvious over **AAAPA** in view of **UGAJIN** and further in view of U.S. Patent No. 5,673,416 to *Chee, et al.* (hereinafter **CHEE**) under 35 U.S.C. § 103(a).

The rejections have been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found among other places on pages 2, 7, 8, and 18-20 of the specification of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. According to the amended claims only one memory is provided which is directly arranged between the two data busses. As such, the input terminal (receive terminal) of this memory is connected to the first data bus and the output terminal (transmit terminal) of the memory is connected to the second data bus.

The amended claims indicate that the single memory device in **UGAJIN** is the buffer memory itself. This buffer memory consists of a receiver buffer and a transmitter buffer whereas the receiver buffer has a settable size depending on the

numbers of the so-called "busy states". In particular, the overall size of the single buffer memory (which contains the transceiver and transmitter buffer) remains the same although the size of the receiver buffer changes. However, the overall size (capacity) of the transmitter buffer area and the receiver buffer area is always constant (col. 2, lines 1 to 3). In contrast, amended claim 1 includes the single memory device that shows no settable size.

In summary, one significant difference between the configuration of the present invention claimed in the instant application and the disclosure provided in **UGAJIN** lies in the type of the used memories. In the present application a single memory, which is advantageously and preferably a FIFO type memory, as recited in new claims 7-9, is used. In contrast to this, **UGAJIN** uses a buffer memory. To increase flexibility, **UGAJIN** discloses partitioning the buffer memory to vary at least the receiver buffer.

In addition, the setting of the size of the memory is made dynamically for a current reading/writing procedure in the instant application. More specifically, since the reading procedure and the writing procedure are coupled with each other in the present invention, dynamic adjustment of the memory is important. To perform an effective reading

procedure with linked memory it is necessary to also provide an effective writing procedure. According to the present invention this is made dynamically for both procedures.

In contrast, the **UGAJIN** reference discloses setting a size of part of the memory (i.e. the receiver buffer) is only performed following on a writing procedure (i. e. a receiving procedure) in said memory. Reading and writing, however, are decoupled in **UGAJIN**. Otherwise the use of a buffer memory would make no sense.

Yet another distinction can be found in the methodology used to dynamically set the size of memory. According to the amended claims, the settable size of the memory is dependent basically on the size of the transmitted data which is written at the same time in this memory. The adjustment of the size of the memory is dynamically performed.

In contrast, **UGAJIN** indicates that setting the size of part of the memory (i.e. the receiver buffer) is only made after the number of empty receiver buffers become smaller than a predetermined number (col. 1, lines 57 to 59). This means that initially the number of busy states has to be counted. After a predetermined time the counted busy states are analyzed and compared with the predetermined number using a table look-up.

After this comparing and analyzing the adjustment of the size of part of the memory (i.e. the receiver buffer) is performed which means that there is no dynamic adjustment of the size since this type of adjustment the results of the comparison and analyzing procedure have to be available.

This is not the case in the instant application, where it is possible to set the size of the available data memory according to the claimed step of dynamically setting the size of the memory. Typically, the memory size according to the instant application is at first set to be small, enabling the memory to be set to the maximum size once the start of a very long data frame is received. This adjustment is being performed **while the data frame is still being transmitted,** that means that the receive procedure is still performed. This is especially useful for very long data frames, where a smaller number of interrupts is triggered by the microprocessor, because the microprocessor has increased the size of the available memory space. Clearly this provides the claimed invention with the special advantage that the performance of the microprocessor is not restricted by too many interrupts.

The use of a FIFO memory as recited in new claims 7-9 is not taught or suggested in the **AAAPA, UGAJIN**, or **CHEE**. For

example, in **UGAJIN** a buffer memory is disclosed which is in its fundamental function and construction completely different to a FIFO type memory. In fact, the applicant respectfully asserts that **UGAJIN** actually teaches away from the use of FIFO memory.

Another difference between the disclosure in **UGAJIN** and the scope of amended claim 1 lies in the provision of a microprocessor controlling the writing and reading process via the first and second data bus and the memory. The Examiner improperly indicates that in **UGAJIN**, "means for executing software sequence" has the same function as a microprocessor. However, this assertion is not correct. More specifically, the means for executing software sequence can also be of the type of a logic unit such as a FPGA (field programmable gate array) or PLD (programmable logic device).

The **AAAPA** reference discloses an HDLC reception line, an HDLC receiver having a large FIFO receiver memory, a microprocessor, a HDLC transmitter having a FIFO transmission memory, and an HDLC transmission line. The HDLC receiver configuration in **AAAPA** only triggers an interrupt signal when the FIFO reception memory is full or if the received D-channel signals include a frame end.

As previously mentioned the length of the D-channel frame varies in both **AAAPA** and the instant application, but in **AAAPA** when the length is longer than the capacity of the FIFO reception memory the interrupt signal will not prompt the microprocessor to receive the data until the FIFO reception memory is full. Since the microprocessor in **AAAPA** will not even start making a response signal until after the microprocessor has read the data, the entire FIFO reception memory must be read before the response data can be written. This delay between reception and transmission in **AAAPA** is sufficient to cause connection difficulties between subscribers.

In contrast, the present invention provides a microprocessor 4 that reads data from variable length data frames from a first data bus 5 and writes the data into a first memory 1. The microprocessor also writes the data in a second memory 9 so that the data can be delivered to a second data bus 7. The amount of data stored in the first memory 1 that will be read out by the microprocessor 4 upon receiving an interrupt is recorded in an RBC register. Subsequently, the microprocessor 4 writes a value that is to be available for the further data reception into an RFBS register. The RFBS register contains the amount of memory needed for the next writing procedure in the memory.

Initially, the memory size of the memory in the instant invention might be adaptively adjusted to be very small and increasingly adjusted by the microprocessor towards the maximum data frame size after receipt of a very long data frame. This configuration increases reliability and decreases connection difficulties, especially when compared with respect to the configuration disclosed in **AAAPA**.

Specifically, the present invention is able to transmit a confirming D-channel signal to a respective subscriber very early and very shortly after the initial receipt of a long data frame, see for example FIG. 3. But the overall number of interrupts is not necessarily increased, because the microprocessor, as a result of the adaptive adjustments through the RFBS register, is able, in the meantime, to increase the available memory space.

While it is clear that this adaptive adjustment process is applicable to the transmission portion of the configuration in FIG. 1 of the instant application, a similar adaptive adjustment cooperation exists between the microprocessor 4 and the second memory 9 and is explicitly described in claim 3 of the instant application.

A second memory control 8, which is associated with the second memory 9, indicates to the microprocessor 4 when the second memory 9 is ready to receive new data. Alternatively, the microprocessor 4 can determine the condition of the second memory 9 through its own query. Once the second memory is ready to receive new data, the microprocessor 4 writes data previously read out from the first memory 1 and adaptively adjusts the size of the second memory 9 for the subsequent writing process of data to a desired value. This adjustment provides the present invention with an optimization of the size of the second memory 9 independent of the size of the data frame that is to be transmitted, another contrast to the constant memory size disclosed in **AAAPA**. In this manner the number of triggered interrupts can be minimized and the efficiency of the microprocessor increased relative to the configuration disclosed in **AAAPA**.

The **UGAJIN** reference discloses a buffer management system for a communication device. An intermediate storage is provided in **UGAJIN** between the transmitting device and receiving device. **UGAJIN thereby pertains to variable partitioning of an intermediate memory between transmitting and receiving devices**. Any such buffering or partitioning is NOT the object of the instant application.

In contrast, the instant application provides an intermediate memory that can receive data frames of variable lengths or sizes and uses an adaptive adjustment of the memory size of the used memory. Exemplary memory devices include a FIFO memory, as indicated in new claims 7-9, where the memory can be dynamically adjusted between two reading processes of the microcontroller. As a result the microcontroller of the instant application can specifically and dynamically adjust the size of the intermediate memory that is to be read by the microcontroller depending on what content the respective data frame has, which is just being written into the memory on the other side of the intermediate memory.

The **CHEE** reference discloses memory request control unit for use in a DRAM interface. Although **CHEE** does include a FIFO module, **CHEE** not teach or suggest using HDLC data frames of variable lengths to transmit data from a first data bus to a second data bus operated asynchronously with respect to the first data bus. Perhaps more importantly, **CHEE** does not overcome the previously discussed deficiencies of **AAAPA** and **UGAJIN**.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1, 3, or 5. Claims 1,

3, and 5 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1, claim 3, or claim 5.

In view of the foregoing, reconsideration and allowance of claims 1-9 are solicited.

In the event the Examiner should still find any of the remaining claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out. In the alternative, the entry of the amendment is requested, as it is believed to place the application in better condition for appeal, without requiring extension of the field of search.

If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith should be charged to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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For Applicant

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